IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	Robert Leinfellner et al.	
Serial No.:	10/598,946	
Filed:	August 31, 2007	Confirmation No. 2387
For:	INFLUENCING DEVICE FOR CONTROL APPARATUS	
Examiner:	Thuy Chan Dao	Group Art Unit: 2192

February 23, 2012

Via: USPTO EFS-Web
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT

Sir:

In response to the Notice of Non-Compliant Amendment dated February 9, 2012, transmitted herewith is an Amendment for the above-identified application.

Amendments to the Claims are reflected in the listing of claims on page 2.

Remarks begin on page 9 of this paper.

AMENDMENTS TO THE CLAIMS

Please replace all prior versions and listings of claims in the application with the listing of claims as follows:

1. (Currently Amended) An adjustment device for adjusting at least one control device with at least one control device microcontroller and with at least one control device debug interface, comprising:

at least one programmable unit comprising a programmable logic chip distinct from the control device microcontroller;

at least one data transmission interface ~~for~~ connecting the adjustment device to an operating unit;

at least one adjustment device debug interface ~~for~~ connecting the adjustment device to the control device debug interface of the control device; and

the at least one programmable unit further comprising at least one memory for at least one address list and at least one data list, where the addresses stored in the address list denote memory locations in the address space of the control device microcontroller and where with the use of the adjustment device debug interface data from the memory locations which are in the address space of the control device microcontroller and which are determined by the contents of the address list can be read and stored in the data list and/or the data stored in the data list can be stored at the memory locations which are in the address space of the control device microcontroller and which are determined by the contents of the address list.

2. (Previously Presented) The adjustment device according to claim 1, wherein the programmable unit comprises the adjustment device debug interface.

3. (canceled)

4. (canceled)

5. (Previously Presented) The adjustment device according to Claim 1, wherein the programmable unit comprises a list application unit and by activation of the list application unit the list application unit automatically carries out either the calling of the data from the memory locations in the address space of the control device microcontroller and given in the address list and the storing of the called data in the data list or the writing of the data stored in the data list into the memory locations in the address space of the control device microcontroller and determined by the contents of the address list.

6. (Previously Presented) The adjustment device according to Claim 5, wherein in the case of several address lists and/or several data lists, by issuing priorities for the address lists and/or data lists a processing order can be determined by the list application unit.

7. (Previously Presented) The adjustment device according to Claim 5, wherein in the case of several address lists and/or several data lists a subset of address lists and/or a subset of data lists can be determined which is processed by the list application unit.

8. (Previously Presented) The adjustment device according to Claim 1, wherein the programmable unit comprises an individual application unit with which any memory locations in

the address space of the control device microcontroller can be read out and/or with which a value can be stored in any memory location in the address space of the control device microcontroller.

9. (Previously Presented) The adjustment device according to Claim 1, wherein the programmable unit comprises a tool interface unit for connecting at least one external device to the adjustment device.

10. (Previously Presented) The adjustment device according to Claim 1, wherein the programmable unit comprises a bypass unit with an associated single-port or dual-port bypass memory, an associated bypass interface for connecting the bypass unit and the bypass memory to an external simulation unit, where data can be exchanged between the control device and the simulation unit with the use of the bypass memory and the bypass unit reading and writing bi-directionally.

11. (Previously Presented) The adjustment device according to claim 10, wherein the programmable unit comprises the bypass interface, where the bypass interface uses a serial data transmission and is embodied as an LVDS interface.

12. (Previously Presented) The adjustment device according to Claim 1, wherein the programmable unit comprises a prioritization and arbitration unit, where priorities can be assigned to the various units of the programmable unit via the prioritization and arbitration unit and the prioritization and arbitration unit determines, with the aid of the priorities assigned to the various units, the order of execution by activation of the various units among themselves and establishes a data connection between the unit activated in each case and the control device.

13. (Previously Presented) The adjustment device according to claim 12, wherein the priority of the bypass unit is higher than the priority of the list application unit and/or that the priority of the list application unit is higher than the priority of the individual value application unit and/or that the priority of the individual value application unit is higher than the priority of the tool interface unit.

14. (Previously Presented) The adjustment device according to claim 12, wherein the priority of the tool interface unit is higher than all the other units.

15. (Previously Presented) The adjustment device according to Claim 1, wherein, the adjustment device comprises a coordination unit which is connected via a coordination interface to one or more of the units of the programmable unit and/or via the data transmission interface to the operating computer and/or via the bypass interface to the simulation unit and/or to the bypass memory.

16. (Previously Presented) The adjustment device according to claim 15, wherein the coordination unit directs data or instructions coming from the operating computer and/or from the simulation unit to the addressed units of the programmable unit for further processing and/or transmits the data coming from a unit of the programmable unit to the operating computer and/or the simulation unit.

17. (Previously Presented) The adjustment device according to Claim 15, wherein the coordination unit provides received data with a time stamp which are transmitted to the operating unit.

18. (Previously Presented) The adjustment device according to Claim 15, wherein the coordination unit interprets configuration instructions coming from the operating unit and/or from the simulation unit and configures the adjustment device accordingly.

19. (Previously Presented) The adjustment device according to Claim 15, wherein the coordination unit registers external trigger signals and/or internal trigger signals and activates corresponding units of the programmable unit.

20. (Previously Presented) The adjustment device according to Claim 15, wherein the coordination unit is located in a separate computer unit outside of the programmable unit, in a microcontroller, in a programmable logic chip, or is formed as a part of the programmable unit.

21. (Withdrawn) A process for adjusting a control device with an adjustment device having at least one control device microcontroller, with at least one control device debug interface, at least one programmable unit, at least one data transmission interface for connecting the adjustment device to an operating unit, at least one adjustment device debug interface for connecting the adjustment device to the control device debug interface of the control device, at least one memory for at least one address list and at least one data list, wherein the programmable unit comprises a bypass unit with an associated single-port or dual-port bypass memory, an associated bypass interface for connecting the bypass unit and the bypass memory to an external simulation unit comprising:

bypassing at least one control device function by a corresponding bypassing function on the simulation unit using, at least in part, the address list and/or the data list.

22. (Withdrawn) The process according to claim 21, wherein

the memory locations of the data necessary for the calculation of the bypass function are stored in the address space of the control device microcontroller in the address list,

the adjustment device automatically carries out the reading of the data from the memory locations which are given in the address list and are located in the address space of the control device microcontroller and the storing of the called data in the data list with the use of the list application unit,

the data stored in the data list are transmitted automatically, or on request by the simulation unit, to the simulation unit,

the results of the calculation of the bypass function by the simulation unit are then transmitted to the adjustment device and stored there either in the data list and/or the bypass memory, and

the results of the calculation of the bypass function from the data list and/or the bypass memory, where those results are stored in the adjustment device, are stored in certain memory locations in the address space of the control device microcontroller, where the memory locations are already stored in the address list or are transmitted by the simulation unit with the results of the calculation of the bypass function.

23. (Withdrawn) The process according to Claim 21, wherein the adjustment device comprises a coordination unit, characterized by the fact that the coordination unit directs data or instructions coming from the operating computer and/or from the simulation unit to the addressed units of the programmable unit for further processing and/or transmits the data coming from a unit of the programmable unit to the operating computer and/or the simulation unit.

24. (Withdrawn) The process according to claim 23, wherein the coordination unit provides received data with a time stamp which are transmitted to the operating unit.

25. (Withdrawn) The process according to Claim 23, wherein the coordination unit interprets configuration instructions coming from the operating unit and/or from the simulation unit and configures the adjustment device accordingly.

26. (Withdrawn) The process according to Claim 23, wherein the coordination unit registers external trigger signals and/or internal trigger signals and activates corresponding units of the programmable unit.

REMARKS

Applicants hereby submit this Amendment in response to the Notice of Non-Compliant Amendment mailed February 9, 2012. Applicant's February 6, 2012 filing included an incorrect version Applicants' amendment. The present filing completely replaces the February 6, 2012 filing. In response to the issue raised by the Notice of Non-Compliant Amendment, the current Amendment includes the text for the withdrawn claims 21-26.

Applicants respectfully request reconsideration of the instant application in view of the amendments, herein, and the following remarks. Claims 1-20 are pending, of which claim 1 is *independent*. Claim 1 is hereby amended. Claims 3 and 4 have been canceled without prejudice. Claims 21-26 were withdrawn by a Response To Election Requirement filed on February 28, 2011.

Claim Rejections - 35 U.S.C. § 102

The Office Action rejected claims 1-20 under 35 U.S.C. § 102(e) as being anticipated by US Patent Publication No. 2004/0054944 A1 to Bates et al. (hereafter Bates). The claims as amended overcome the pending rejection. Applicants hereby respectfully request allowance of the pending claims.

Bates discloses a software debugger for a typical computer system:

> The present invention generally relates to computers and computer software. More specifically, the invention is generally related to determining thread termination in a debugging environment.

Bates Para. 0002. Moreover, the *software* debugger application disclosed by Bates debugs software running on the same computer as the software debugger. *See, e.g.*, Paras. 0028 and 0033.

The Examiner asserts that:

- the adjustment device in Bates is the entire Computer System 10,
- the control device in Bates is the Processor 12 and Debug User Interface 24 of Computer System 10, and
- the adjustment device memory in Bates is memory 16 of Computer System 10.

These features of Bates identified by the Examiner are all part of the same Computer System 10 and run on the same processor 12. Thus, as the Examiner acknowledges, the pending rejection was premised on a reading of Bates such that the adjustment device and control device are the same Computer System 10 having processor 12. (See, 11/07/2011 Office Action at 2).

In contrast to the single computer system debugger disclosed by Bates, independent claim 1 of the present application recites an adjustment device having:

> at least one programmable unit comprising a programmable logic chip distinct from the control device microcontroller;
>
> the at least one programmable unit further comprising at least one memory for at least one address list and at least one data list,

Claim 1 recites that the adjustment device adjusts comprises "at least one programmable unit comprising a programmable logic chip distinct from the control device microcontroller." Thus, claim 1, as amended, requires the programmable unit of the claimed adjustment device to include a programmable logic chip distinct from the processor of the control device that it is debugging. This arrangement has the advantage of reducing the resources of the control device that need to be used during debugging. *See*, ¶¶ 17 and 30 of Applicant's specification. In contrast, Bates discloses the debugging and the system being debugged running on the same computer system and processor.

Claim 1, as amended, also requires "the at least one programmable unit further comprising at least one memory for at least one address list and at least one data list." Accordingly, the memory holding the address list and data list is within the programmable unit of the adjustment device, not the control device. In contrast, the memory cited in Bates is part of the alleged control device being debugged. The claimed system, thus, has the advantage of reducing the use of the memory of the control unit for debugging purposes.

The advantages of the invention of claim 1 are particularly useful for the debugging of embedded systems. Embedded control units are often designed to have just enough memory and other hardware specifications to run perform as required in the final production environment. That means that control unit very little memory or other computing resources available for the debugging processes required during the development and testing phase of product design. Increasing the memory and system resources in the control unit merely for the sake of debugging will have the disadvantageous result that the multitude of control units in the final product will have more memory or other resources than is necessary, which would increase costs. The adjustment device of claim 1 improves this situation by offloading some of the debugging processing and memory requirements to the adjustment device.

In view of the express limitations of amended claim 1, Bates does not anticipate Claim 1 and the pending rejection should be withdrawn. The above-discussed distinction also applies to claims 2, and 5-20, which depend, directly or indirectly, from claim 1. In view of the foregoing, Applicants respectfully request withdrawal of the pending rejections and allowance of the pending claims.

CONCLUSION

Consequently, the reference cited by the Office Action do not disclose in the claimed invention. Thus, the Applicants respectfully submit that the supporting remarks and claimed inventions, claims 1-2, 5-20, all: overcome all rejections and/or objections as noted in the office action, are patentable over and discriminated from the cited reference, and are in a condition for allowance. Furthermore, Applicants believe that the above remarks, which distinguish the claims over the cited reference, pertained only to noted claim element portions. These remarks are believed to be sufficient to overcome the prior art. While many other claim elements and/or bases for rejection were not discussed as they have been rendered moot based on the above remarks, Applicants assert that all such remaining and not discussed claim elements and/or bases for rejection, all, also are distinguished over the prior art and reserves the opportunity to more particularly traverse, remark and distinguish over any such remaining claim elements and/or bases for rejection at a later time should it become necessary. Further, any remarks that were made in response to an Office Action objection and/or rejection as to any one claim element, and which may have been re-asserted as applying to another Office Action objection and/or rejection as to any other claim element(s), any such re-assertion of remarks is not meant to imply that there is commonality about the structure, functionality, means, operation, and/or scope of any of the claim elements, and no such commonality is admitted as a consequence of any such re-assertion of remarks. As such, Applicant does not concede that any claim elements have been anticipated and/or rendered obvious by any of the cited reference. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection and allowance of all claims.

AUTHORIZATION

Applicant hereby authorizes and requests that the Commissioner charge any fee or credit any overpayment for such an extension of time to Deposit Account No. 15-0665, Order No. 020301-004007.

Reconsideration of the above-identified application is respectfully requested.

Respectfully submitted,

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